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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,065	02/02/2004	Shigetaka Aoki	60188-740	6161

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/768,065	AOKI ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/326,059.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/2/04; 5/19/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent Publication 2001-319935 to Shiono et al. (cited by applicant).

Regarding claim 1, Shiono discloses a semiconductor device (figure 1) comprising: a single crystalline underlying layer (3, 4 paragraph 0021) formed in part of a substrate (1,3); an insulating layer (6; paragraph 0022) formed in another part of the substrate (figures 1, 2c); a semiconductor layer (10) epitaxially grown above the underlying layer (paragraph 0024) having a composition intersecting the claimed range (see paragraph 0023); a buffer layer (9) epitaxially grown (see paragraph 0024) between the underlying layer and semiconductor layer (figure 1) and having a composition intersecting the claimed range (see paragraph 0023), where the buffer layer has a greater quantity of Si than the semiconductor layer (see paragraph 0023; buffer layer has as

Ge composition of 0-0.05, whereas the semiconductor layer has a Ge composition of 0.05-1); and a polycrystalline semiconductor layer formed on the insulating layer and having the same composition as the buffer layer (portion of 9 on layer 6) and semiconductor layer (portion of 10 on layer 6; also see paragraph 0026 – portion of 9 and 10 in window = single crystal semiconductor, and portion on insulating layer 6 = polycrystalline semiconductor).

Regarding claim 2, Shiono discloses that the single crystalline underlying layer is Si (3; paragraph 0021).

Regarding claim 3, Shiono discloses that the semiconductor layer and polycrystalline layer are SiGe (10; paragraphs 0023-0026), the buffer layer is a Si layer (layer 9 includes x=0 condition, which corresponds to a pure Si layer; see paragraphs 0023-0026; 0033).

Regarding claim 4, Shiono discloses that the underlying layer is a collector layer (layer 3, including regions 4 and 5, acts as a collector – see description of notations section; the semiconductor layer has at least part serving as a base layer (11) and wherein the polycrystalline semiconductor layer serves as at least part of a base lead electrode (see figure 1; polycrystalline portion (left-most portions of layer 10) connects base region and base electrode (20)), the device functioning as a heterojunction bipolar transistor (see paragraphs 0019, 0021, etc).

Regarding claim 6, Shiono discloses a buffer layer thickness intersecting the claimed range (paragraph 0024).

3. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by Japanese Patent Publication 2002-026027 to Yokoyama et al (cited by applicant).

Regarding claims 1-3, Yokoyama discloses a semiconductor device (figure 6) comprising: a single crystalline underlying silicon layer (112, 113; paragraph 0011) formed in part of a substrate (111, 112; see figure 6); an insulating layer (110) formed in another part of the substrate (paragraph 0011); a semiconductor layer (132) epitaxially grown (paragraph 0014) above the underlying layer and being formed of SiGe (paragraph 0014); a buffer layer (121) epitaxially grown between the underlying layer and semiconductor layer, having a Si composition (paragraph 0014); and a polycrystalline semiconductor layer (133, 122) formed on the insulating layer (figure 6) and having the same composition as the buffer layer (portion 122; see paragraph 0014) and a semiconductor (133) having the same composition as the semiconductor layer (paragraph 0014).

Regarding claim 4, Yokoyama discloses that the underlying layer is a collector layer (paragraph 0012; layers 113 and 131 form collector); the semiconductor layer has at least part serving as a base layer (paragraph 0012 – layers 121 and 132 form the base region); and wherein the polycrystalline layer serves as part of a base lead electrode (portion 133) connects base to the base electrode (see paragraph 0013), the device functioning as a HBT (see paragraph 0019; device is a BJT using Si/SiGe heterojunctions, and thus is a HBT.

Regarding claim 6, Yokoyama discloses that the buffer layer thickness is 10 nm (paragraph 0014).

4. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,551,891 to Chantre et al.

Regarding claims 1-3, Chantre discloses a semiconductor device (figure 12) comprising: a single crystalline Si underlying layer (4; column 4, lines 10-14) formed in part of the substrate (figure 1); an insulating layer (5) formed in another part of the substrate (figure 1); a semiconductor layer (81) with a SiGe composition (column 4, lines 60-65) epitaxially grown above the underlying layer; a buffer layer (80) formed of Si, epitaxially grown (column 4, lines 59-61) between the underlying layer and the semiconductor layer; and a polycrystalline semiconductor layer formed on the insulating layer (column 5, lines 4-11), having a portion with the same composition as the buffer layer (portion of 80 over 5 and 17) and a portion with the same composition as the semiconductor layer (portion of 81 over 5 and 17).

Regarding claim 4, Chantre discloses that the underlying layer is a collector layer (column 4, lines 29-31), the semiconductor layer is a base layer (column 4, lines 55-67); and the polycrystalline layer serves as a base lead electrode (figure 12), the structure functioning as a HBT (structure is a bipolar transistor – figure 12 – having a Si/SiGe heterojunction).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chantre et al. in view of Shiono et al.

Chantre discloses that the device functions as a BiCMOS device (column 4, lines 30-37), where an oxide layer acting as the gate oxide of a MIS transistor is formed immediately prior to the Si/SiGe layer deposition.

Chantre fails to specifically teach that the polycrystalline layer forms part of the gate electrode of the MIS transistor.

Shiono teaches that the same deposition step for the base formation of a HBT can be used for depositing a polycrystalline Si/SiGe gate electrode for a MIS transistor (see paragraph 0036).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the gate electrode of the BiCMOS device of Chantre is formed from the polycrystalline SiGe layer of the HBT, as suggested by Shiono. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use the polycrystalline semiconductor layer as the gate electrode of the MIS transistor, because doing so allows the base region of the HBT, the base lead electrode of the HBT, and the gate electrode of the MIS to be formed in the same process step, which decreases the complexity of fabrication, as is appreciated by a person skilled in the art.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,900,115 to Todd discloses SiGe deposition on mixed-morphology substrates.

b. U.S. Patent No. 5,356,821 to Naruse et al. discloses a BiCMOS using the same step for depositing the gate electrode of the MOS transistor and the base region of the HBT.

c. U.S. Patent No. 6,563,147 to Ikeda and U.S. Patent No. 6,346,453 to Kovacic et al. disclose Si/SiGe HBTs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

LAURA M. SCHILLINGER
PRIMARY EXAMINER